U.S. Navy Study Proves Effectiveness of EMS Heat Control Technique

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The Science of Component Heat Damage

Most modern electronic components fail because of heat damage suffered during hand soldering or repair. Once internal temperatures exceed roughly 450°F/232°C, damage begins and the rate of decay accelerates quickly as the temperature increases. For more information, please go to http://www.emsciences.com/heat-control.html

So, how can we prevent heat damage when soldering iron temperatures exceed 450° by at least a couple of hundred degrees? Is it even possible?

In the early days of electronics, metal clamps called "heat sinks" were placed on component leads between the soldering iron and the heat–sensitive component body. Heat was drawn into the heat sink rather than reaching the component body. But, as components shrank, there was no longer room for heat sinks.

The U.S. Navy's High Reliability Soldering Method

In recent decades, the U.S. Navy's technique of soldering leads in a solder pot then quickly reflowing the leads to the circuit board has been considered the ultimate in high reliability soldering. The solder pot temperature is low and the soldered leads can be reflowed quickly, minimizing the time that the iron is in contact with the component. This technique works; it does prevent the heat damage caused by the technique found in all solder training for the past 60 years. However, the technique is not perfect. In particular:

1. Solder pots are big and somewhat dangerous
2. Not everyone has a solder pot
3. The solder pot method involves extra steps and time
4. Dipping fine–pitch multileaded surface mount parts generally results in serious bridging

Basically, the Navy approach is not practical for commercial manufacturing. There must be a better way. We set out to find it.

Our High Reliability Soldering Method

We developed a simple technique that keeps the component temperature in the safe range even if using an 800° iron. The technique works with any iron, requires no additional tools or materials and is just as fast and easy as the soldering technique everyone has been using since the days of vacuum tubes.

The U.S. Navy commissioned a laboratory analysis comparing the intermetallic created by our technique to the intermetallic created with the Navy's technique. Intermetallic — the combination of tin from solder and the metal being soldered — reflects the amount of heat injected during the soldering. Thicker intermetallic means that more heat was injected; less heat translates into thinner intermetallic.

The Test

The experiment consisted of soldering bare copper wire to tin–plated turret terminals.

U.S. Navy soldering instructors soldered their wires to a series of turret terminals (designated by the laboratory in its report as Boards 1 and 2) using the following steps:

1. Apply flux to the bare copper
2. Insert the wire into a solder pot
3. Remove the wire from the solder pot
4. Wrap the wire on terminal
5. Reflow the wire to the terminal using flux–cored solder

We soldered wires to other terminals (Boards 3 and 4) using these steps:

1. Apply flux to the bare copper
2. Wrap the wire on terminal
3. Solder to the terminal using flux–cored solder and our heat control technique. To show the effectiveness of our heat control technique, we applied extra solder, meaning the iron was in contact with the parts longer than necessary.

The laboratory cross–sectioned solder connections from the Navy–produced product and ours. The intermetallic layers of the samples were then compared visually and electronically.

The Results

Not knowing the processes that had created the connections, the laboratory incorrectly concluded that all the wires "seemed to be 'pre–Tinned' before soldering." ("Pre–Tinning" or just "Tinning" is a term often used for the process of soldering the component in a solder pot before reflowing it to the final assembly.) However, only the Navy's units (Boards 1 and 2 in the report) were pre-Tinned.

The laboratory noted that the solder on the units soldered using our technique (i.e., Boards 3 and 4 where the wires were not pre-Tinned) is rougher and there is "bare copper where the solder did not fully wet the wire. This was not seen on every turret but was visible on approximately half of the soldred turrets." The rougher appearance is the result of differences in the fluxes; the Navy used a rosin flux which was removed after soldering while we used an organic no–clean flux that was not removed. The exposed copper is located at the point where the soldering iron touched the wire during soldering; because the iron was very hot (800°) to demonstrate the effectiveness of the heat control technique, the flux around the iron burned off and the copper reoxidized before the solder reached that area.

The critical result is the comparison of intermetallic layers. The laboratory found that: "the intermetallic layer formed at the boundary between solder and copper, and the solder and brass, is relatively the same thickness" on all of the samples. In other words, **our simple heat control technique provides the same protection against overheating as the more complicated and expensive technique used by the U.S. Navy**.

The Electronics Manufacturing Sciences' heat control technique is only available through Science of Soldering. No other soldering course teaches how to prevent heat damage to components.

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Solder Comparison on Turret Style Test Vehicles

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Statement of Work

Four test boards containing eight turrets were received from Crane Division, Naval Surface Warfare Center for solder evaluation. Two turrets from each board were cross-sectioned and then analyzed at both SAIC (Merriville, IN) and Purdue University (West Lafayette, IN) for visual and microstructural differences.

Sample Preparation

Turrets were isolated from the board by cutting the glass/epoxy board using metal shears. Each turret was then cut slightly off center according to *Figure 1* using a Buehler Isomet low speed saw. Each turret was cut off center to account for material lost during grinding. The specimens were then cleaned using soap and water then dried to remove oil residue. Two specimens were then set in Buelhler Epoxicure resin and harder. Epoxicure was used because it sets at a low temperature and would not change the "as received" metallurgy. The mounted specimens were then ground/polished by hand using a LECO Spectrum 1000 and 400, 600, 1200 grit SiC grinding wheels. Special attention was given while grinding to ensure that each specimen would represent a cross-section cut down the center of the turret. The samples were cleaned using distilled water between each grit size progression. The samples were polished on cloth using 0.05 µm Alumina from Buehler and distilled water mixture. Colloidal Silica was then used to polish and etch the solder to enhance the microstructure. Distilled water and ethanol were used to clean and dry the samples after each fine polishing step. The final polished mounted sample is pictured in *Figure 2*. The samples were investigated using optical and electronic microscopy highlighted in *Figure 3*.

FIGURE 1 *(left)* Isomet low speed saw by Buelher. (www.buelher.com) *(center)* Area removed using Isomet saw. *(Right)* LECO Spectrum 1000 (www.purdue.edu/mse)

FIGURE 2 Polished sample holding two turret cross-sections.

FIGURE 3 *(left)* Olympus SZX7 stereoscope *(center)* Olympus GX51 inverted microscope and *(right)* Hitachi TM-1000 tabletop SEM.
(Olympus images from www.purdue.edu/mse and TM-1000 from SAIC, Merriville, IN)

Analysis

Pre-Analysis

Before the samples were sectioned, they were inspected to investigate the samples history. A XRF was used to determine that the turrets were brass with a layer of pure Tin. It appeared that the brass turrets had been "dipped" in Tin before soldering. The wire that was soldered to the turret was pure copper but also seemed to be "pre-Tinned" before soldering.

Solder Volume and Appearance

After inspecting each turret using stereomicroscopy, it was evident that boards 1 and 2 were processed different from 3 and 4 based on solder finish and volume. While the volume and finish of solder does not affect the bonding strength between the turret and the wire, it is worth noting that there are differences between boards 1 and 2 vs. boards 3 and 4. *Figure 4.a* shows a turret from board 2 that is representative of the turrets on boards 1 and 2. *Figure 4.b* is a turret on board 4 that shows excess solder volume and a rougher solder finish which is consistent with all the turrets on boards 3 and 4. The wire wrapped around the turret in *Figure 4.b* shows bare copper where the solder did not fully wet the wire. This was not seen on every turret, but was visible on approximately half of the soldered turrets on boards 3 and 4. *Figure* 5 shows SEM images of the cross-sections from each board. The images support the fact there is excess solder on boards 3 and 4.

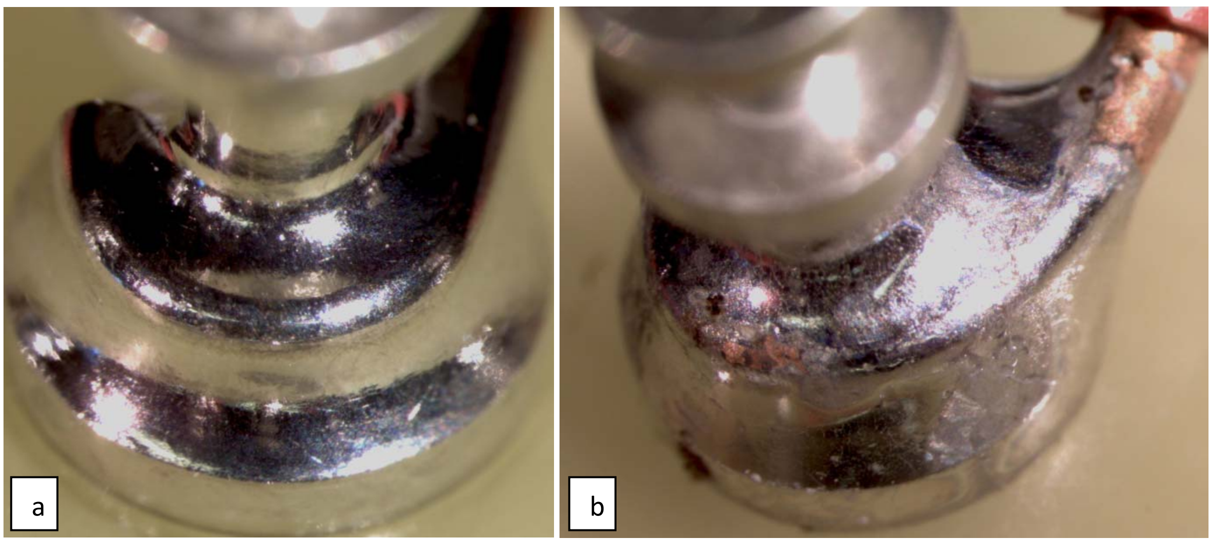

FIGURE 4 *a.)* Turret from board 2 *b.)* Turret from board 4.
Images from stereoscope at magnification approximately 30 – 45x

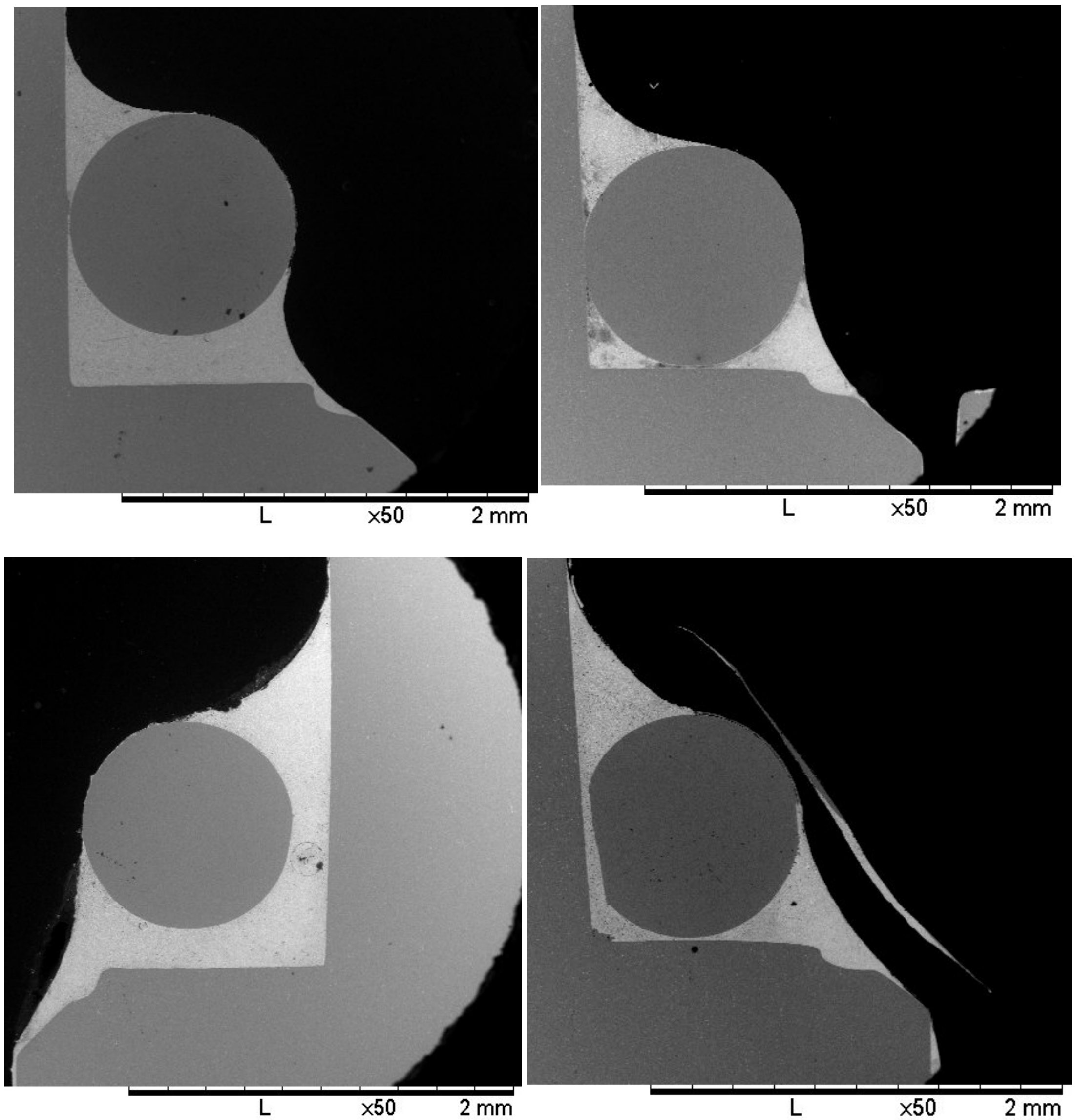

FIGURE 5 SEM images of solder cross-sections on *(top left)* board 1, *(top right)* board 2, *(bottom left)* board 3 and *(bottom right)* board 4

Intermetallic at Boundaries

After two turrets from each board were cross-sectioned and polished, they were inspected using backscatter electron SEM. *Figure 6* compares two images obtained from the SEM and processed using the Hitachi SEM software. As seen in *Figure 6*, the intermetallic layer formed at the boundary between solder and copper, and the solder and brass, is relatively the same thickness. Throughout boards 1, 2, 3, and 4, the thickness is approximately one micron and ranges from 0.7 µm to 1.2 µm within a single specimen.

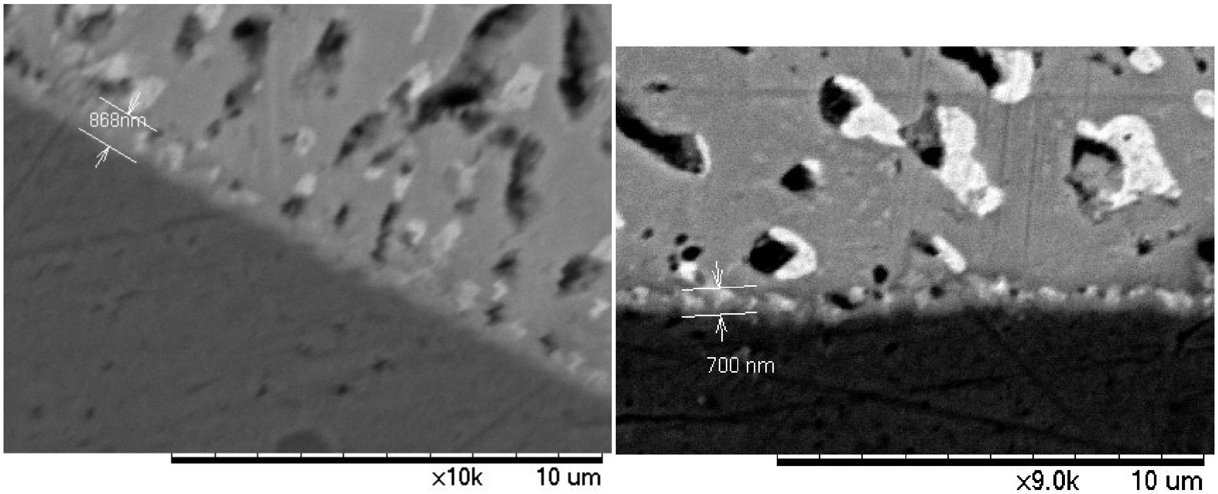

FIGURE 6 (*left)* Solder-copper interface and *(right)* solder-brass interface of cross-section of turret on board 3. Images were taken using BSE SEM and processed using Hitachi SEM software.

Bulk Intermetallic

While soldering a small amount of Copper can melt and mix with the solder resulting in an intermetallic (Cu_6Sn_5) within the bulk microstructure. *Figure 7* shows such an intermetallic present in turrets from board 1. Board 2 shows a small amount of this intermetallic but almost negligible. Boards 3 and 4 show no bulk intermetallic. The difference in amount of copper dissolved into the microstructure between boards 1 and 2 could be attributed to operator variance. The lack of bulk intermetallic in boards 3 and 4 could be due to the operator or processing.

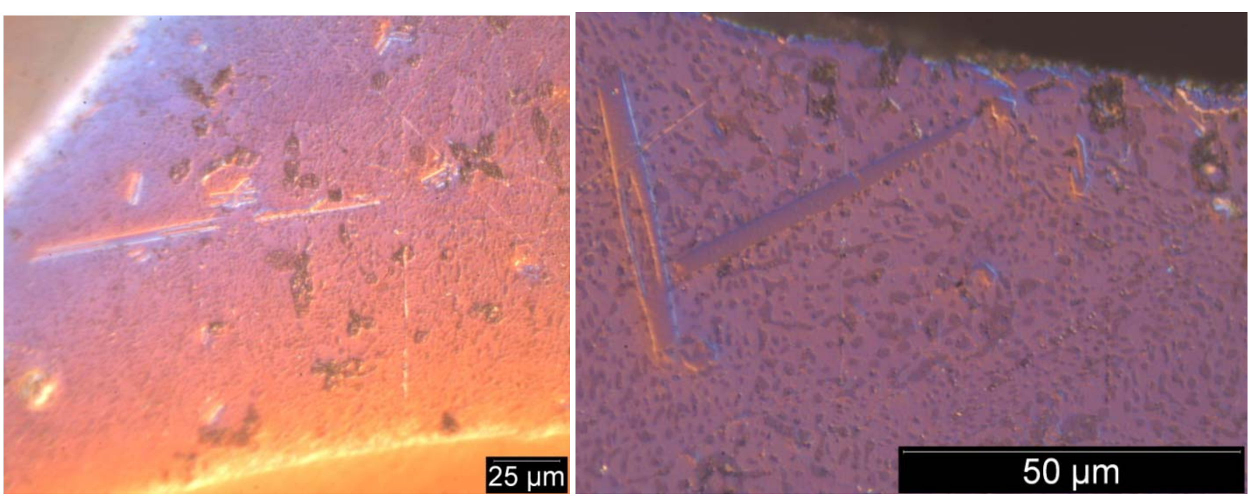

FIGURE 7 Optical micrograph of Cu_6Sn_5 intermetallic within eutectic Sn-Pb solder on turret on board 1.

Grain Size and Structure

The grain size and structure of the solder were relatively constant between all the boards. Micrographs from each board showed Lead dendrites where lead rich areas solidified before the eutectic grains formed. *Figure 8* shows a comparison between boards.

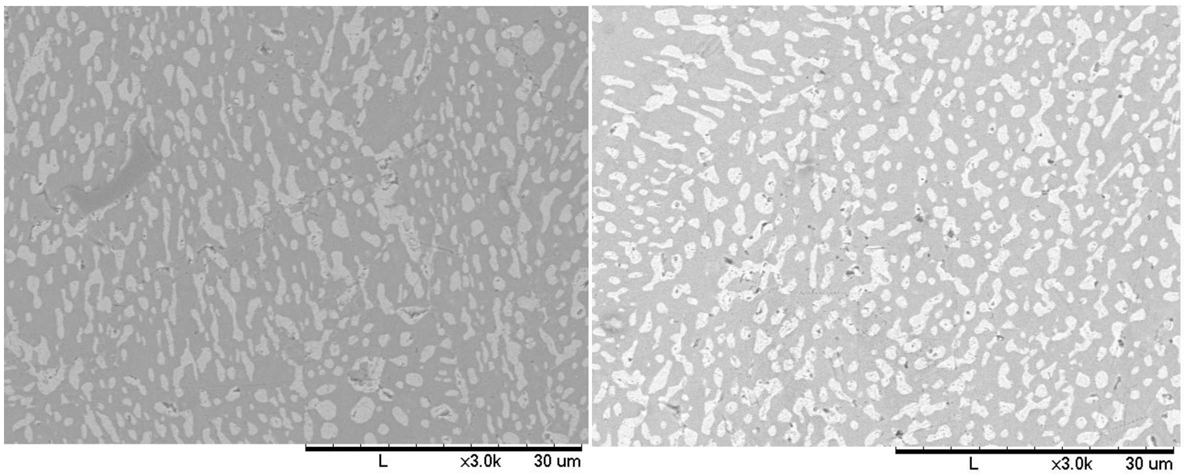

FIGURE 8 Micrographs of Eutectic SnPb on *(left)* board 1 and *(right)* board 4.

Discussion

After first inspection, it was clear that boards 1 and 2 either had a different operator or they were processed differently than boards 3 and 4. The differences were in appearance and solder volume, which should not affect the solders bonding characteristics. When the turrets were cross-sectioned, the grain size and intermetallics at the interfaces were consistent between each board. The only difference in intermetallics was that board 1 had more bulk intermetallic than board 2, while boards 3 and 4 had no bulk intermetallic. The amount of solder used on boards 3 and 4 may have masked some microstructure features like bulk intermetallics. For future testing, more realistic, smaller components should be used as test vehicles. The four boards received from NSWC Crane were similar in intermetallic thickness and microstructure but differed greatly in aspects, which relate to the operator, such as solder volume and appearance.